A CMOS DCCII with a Grounded Capacitor Based Cascadable All-Pass Filter Application

Bilgin METIN[1], *Norbert HERENCSAR*[2], *Kamil VRBA*[2]

[1]Dept. of Management Information Systems, Bogazici University, Hisar Campus, 34342 Bebek-Istanbul, Turkey
[2]Dept. of Telecommunications, Brno University of Technology, Purkynova 118, 612 00 Brno, Czech Republic

bilgin.metin@boun.edu.tr, herencsn@feec.vutbr.cz, vrbak@feec.vutbr.cz

Abstract. *The differential current conveyor (DCCII) is a versatile current-mode active element, which has a current differencing capability. In this study, a new CMOS DCCII implementation is introduced. As an application example, a novel voltage-mode (VM) first-order all-pass filter (APF) is presented. The proposed VM APF employs two resistors, grounded capacitor and has high-input impedance for cascadability. Simulation and experimental results are given to verify the operation of the circuit.*

Keywords

All-pass filter, analog filter, differential current conveyor, DCCII, voltage-mode circuit.

1. Introduction

An all-pass filter (APF) is a special type of filter, which can modify the phase of the input signal while keeping its amplitude constant. For the voltage-mode (VM) APFs high-input impedance is important, if these circuits are used as a load to another analog filter in the signal-processing path for compensating phase shifts. Due to this property, there is no need for an additional buffer or current conveyor (CC) for cascading and it decreases the number of active elements in the design. In the current technical literature, several VM first-order APFs were proposed employing various high-performance active building blocks (ABBs) [1]–[16], [18]–[21]. These filters have different useful properties depending on the individual circuit as they are summarized in Tab. 1. For example, the all-pass filters based on the second-generation current conveyor (CCII) in [1] and [6] employ a grounded capacitor, but they do not have a high-input impedance property and the circuit in [1] has disadvantage of using three resistors. The all-pass filters in [2]–[5] employing single second- or third-generation CC do not have a grounded capacitor and they are not cascadable. Two cascadable all-pass filters with high-input impedance feature were proposed using single minus-type CCII in [7], but they use a floating capacitor and three resistors. The circuits in [8] and [9] are based on the dual-output CCII and modified CCII, respectively, enjoy having both high-input impedance and grounded capacitor. Also circuits in [10]–[15] have both high-input impedance and grounded capacitor, but only filters in [10], [12]–[14] provide low-output impedance feature simultaneously. The filter in [10] includes two differential voltage CCs (DVCCs) and circuits in [11]–[13] employ two differential difference CCs (DDCCs). The circuits in [14] and [15] employ fully differential CC (FDCCII). As drawback of solutions [12] and [13] the usage of four or three passive elements can be mentioned, respectively, but all in grounded form. The circuit in [16] with a grounded capacitor and single DDCC only provides low-output impedance. In the literature [17] different kinds of ABBs exist and those are also used in the design of all-pass filter circuits. The circuit in [18] is cascadable and has a grounded capacitor, but the active element called voltage differencing-differential input buffered amplifier (VD-DIBA) is an interconnection of two active elements such as an operational transconductance amplifier and differential input voltage buffer. Hence, it may includes large number of transistor. All-pass filters in [19]–[21] using single current-controlled current differencing buffered amplifier (C-CDBA), current-controlled inverting CDBA, or universal voltage conveyor (UVC), respectively, have floating capacitor and low-output impedance feature. Unfortunately, from these three referred circuits only the UVC-based APF in [21] features with high-input impedance simultaneously.

In addition to above listed ABBs, the differential current conveyor (DCCII) was introduced in 1996 [22] as the first current-mode active element with current differencing capability. However, in the literature it has not received as much as attention than the conventional CDBA presented in 1999 [23]. In fact, the DCCII combines the simplicity of the classical CCII [24] with current differencing feature of the CDBA. Therefore, the DCCII looks like a CDBA for current differencing operation, but it has an additional voltage terminal like CCII, which has high-input impedance and can be useful for cascading VM circuits. In addition, the DCCII includes fewer numbers of transistors than CDBA, which has a supplementary voltage buffer stage. In this study, to increase the variety of DCCII circuits in the literature, its novel implementation using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm level-3 [25] CMOS process parameters is proposed. High-input impedance feature

Reference	ABB type[#]	No. of ABBs	No. of transistor	No. of resistors	Grounded capacitor	No matching constraints	High-input impedance	Low-output impedance
[1]	CCII+	1	*X*	3	yes	no	no	no
[2]	CCII–/CCCII–	1	*D*	2/1	no	no	no	no
[3]	CCIII–	1	24*	3/2	no	no	no	no
[4]	CCII+	1	*D*	2	no	no	no	no
[5]	CCII–/CCCII–	1	*D*	2/1	no	no	no	no
[6]	CCII–/CCCII–	1	13*	2/1	yes	no	no	no
[7]	CCII–	1	*X*	3	no	no	yes	no
[8]	DO-CCII	1	23*	2	yes	no	yes	no
[9]	MCCII–	1	21*	2	yes	no	yes	no
[10]	DVCC+	2	24	1	yes	yes	yes	yes
[11]	DDCC	2	44	0	yes	yes	yes	no
[12]	DDCC+	2	24	3	yes	yes	yes	yes
[13]	DDCC+	2	24	2	yes	no	yes	yes
[14]	FDCCII	1	36*	1	yes	yes	yes	yes
[15]	FDCCII	1	44*	1	yes	yes	yes	no
[16]	DDCC+	1	18	1	yes	yes	no	yes
[18]	VD-DIBA	1	*D*	0	yes	yes	yes	yes
[19]	C-CDBA	1	37*	1	no	no	no	yes
[20]	C-ICDBA	1	30*	0	no	no	no	yes
[21]	UVC	1	40*	2	no	no	yes	yes
Proposed - simulated	DCCII	1	21*	2	yes	no	yes	no
Proposed - measured	DCCII	2	*D*	2	yes	no	yes	yes

Tab. 1. Comparison of previously published VM all-pass filters (Note: [#] Refer Appendix for nomenclature of the ABBs, * Ideal current sources assumed, *X* Simulations or experiments not provided, *D* Direct ICs used).

of the DCCII is with advantage used in a novel cascadable VM first-order APF design as an application example. The proposed circuit includes a single DCCII, a grounded capacitor, and two resistors. Here it is worth mentioning that, similarly to the circuits in [6], [8], [9], [13], the proposed circuit includes a grounded capacitor in series to X terminal, which may affect the high frequency behavior of the filter. In addition, analogous to circuits in [1]–[9], [13], [19]–[21], the proposed circuit requires a simple resistor matching condition. Note that in the current integrated circuit (IC) technologies it is possible to match resistors with much better precision than 0.1 % [26]. Although these new IC technologies also offer floating capacitor realization possibility as a double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor [27], widely accepted are those filters that employ only grounded capacitors. Compared to floating counterparts, grounded IC capacitors have less parasitics that can be significant from the performance standpoint. In the introduced APF both resistors are in series to X terminals, which is an advantage, because unwanted effects of the parasitic resistances at X terminals can be compensated by choosing sufficiently high resistor values. In addition, due to the high-input impedance of the circuit there will be no need for an additional buffer or CC for cascading and this will decrease the number of active elements in the design. The theoretical results are verified by SPICE simulations and the behavior of the proposed circuit is also experimentally measured using the readily available current feedback amplifiers (CFAs) AD844 ICs produced by the Analog Devices, Inc. Thanks to the voltage buffer in the output part of the CFA used in experiments, the proposed APF also has low-output impedance, and therefore, it is fully cascadable.

2. The DCCII and Proposed CMOS Implementation

The differential current conveyor (DCCII) [22] is a four-terminal ABB and its circuit symbol is shown in Fig. 1(a). The difference of the currents at the X_P and X_N terminals are reflected to the Z terminal. The potential of the Y terminal is copied to the X_P and X_N terminals. Considering the non-idealities caused by the physical implementation of the DCCII, the relationship between port currents and voltages can be described by the following hybrid matrix:

$$\begin{bmatrix} v_{XN} \\ v_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_N \\ 0 & 0 & \beta_P \\ \alpha_P & -\alpha_N & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ v_Y \end{bmatrix} \tag{1}$$

where ideally $\beta_N = \beta_P = 1$ and $\alpha_N = \alpha_P = 1$ that represent the voltage and current transfer ratios of the DCCII, respectively.

The realization of the CMOS DCCII shown in Fig. 1(b) was derived from the C-CDBA/C-ICDBA and CCCII structures presented in [19], [20], and [28], respectively. In Fig. 1(b), transistors M_1–M_4, M_{18}, and M_{19} realize a mixed translinear loop, which transfers Y terminal potential to both X_N and X_P terminals. Transistors M_5–M_{10} and M_{12} provide biasing for the mixed translinear loop. Transistors M_{11}, M_{13}–M_{19}, M_{20}, and M_{21} form a current differencing circuit at the Z terminal for the input currents flowing in to the X_N and X_P terminals.

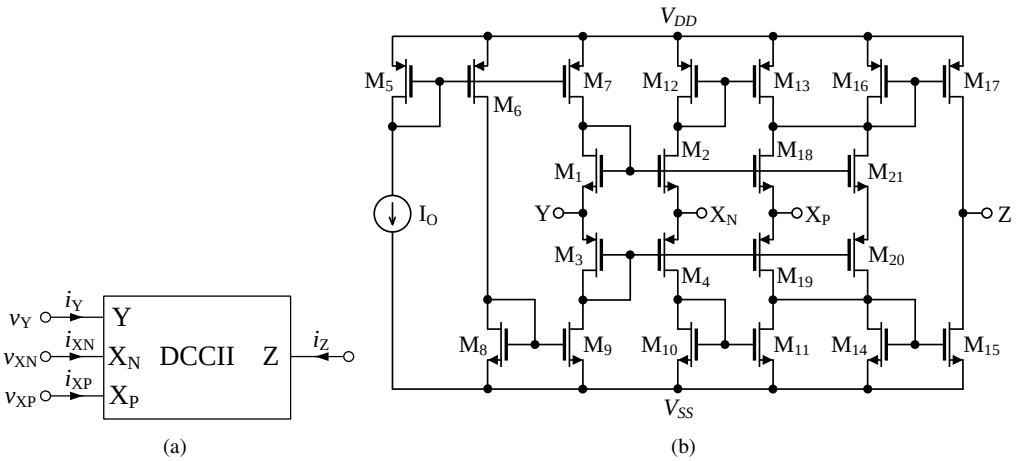

Fig. 1. (a) Circuit symbol of DCCII and (b) its proposed CMOS implementation.

3. Application Example: A Cascadable All-Pass Filter with Grounded Capacitor

The proposed first-order all-pass filter using a single DCCII, two resistors, and one grounded capacitor is shown in Fig. 2. Its voltage transfer function can be expressed as:

$$\frac{V_o}{V_i} = \frac{2+2sCR_1 - sCR_2}{2+2sCR_1}. \tag{2}$$

Here it should be emphasized that the presented circuit has resistors in series to its X terminals. Hence, by selecting sufficiently high values of R_1 and R_2 the unwanted effects of the parasitic resistors at the X terminals to the operation and resistor matching condition of the circuit can be easily compensated. Assuming $4R = R_2 = 4R_1$, (2) reduces to:

$$\frac{V_o}{V_i} = \frac{1-sCR}{1+sCR}. \tag{3}$$

Considering non-idealities given in (1), the following transfer function is obtained:

$$\frac{V_o}{V_i} = \frac{(1+\alpha_P)\beta_P + (1+\alpha_P)\beta_P sCR_1 - \alpha_N\beta_N sCR_2}{(1+\alpha_P) + sCR_1(1+\alpha_P)}. \tag{4}$$

For a known current and voltage gain values, a resistor matching value of k ($R_2 = kR_1 = kR$) can be obtained that can compensate for effect of active element non-idealities as follows:

$$k = \frac{2\beta_P(1+\alpha_P)}{\beta_N\alpha_N}. \tag{5}$$

The parasitics in the physical realization of the current conveyors limit the high frequency of operation. Therefore, the $\alpha(s)$ and the $\beta(s)$ are respectively the current and voltage transfer ratios of the DCCII and they can be described by the following first-order functions:

$$\alpha_{N,P}(s) = \frac{\alpha_0}{1+s\tau_\alpha}, \quad \beta_{N,P}(s) = \frac{\beta_0}{1+s\tau_\beta} \tag{6}$$

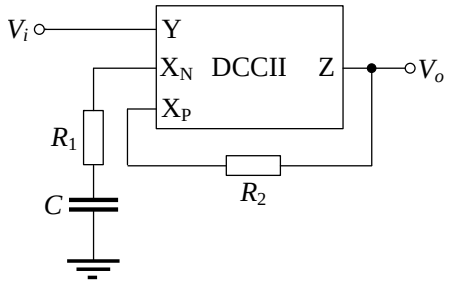

Fig. 2. The proposed first-order all-pass filter employing a DCCII.

where the α_0 and β_0 are the values of the current and the voltage transfer ratios and $\omega_\alpha = 1/\tau_\alpha$ and $\omega_\beta = 1/\tau_\beta$ represent their corresponding poles. Here for simplicity, the current and voltage gains at low frequencies are assumed to be equal to α_0 and β_0, respectively. Combining (6) with non-ideal transfer function in (4) for $4R = R_2 = 4R_1$, the frequency dependent transfer function of the presented circuit can be expressed as follows:

$$\frac{V_o(s)}{V_i(s)} = \beta_0 \frac{(1+s\tau_\alpha)(1+sCR) + (1-3sCR)\alpha_0}{(1+sCR)(1+s\tau_\beta)(1+\alpha_0+s\tau_\alpha)}. \tag{7}$$

Equation (7) shows that the presented circuit can still work as first-order all-pass filter for $\{\tau_\alpha, \tau_\beta\} \ll CR$ and there is no stability problem due to the frequency dependency of the current and voltage gains.

4. Simulation Results

To verify the theoretical analyses, the proposed CMOS DCCII implementation in Fig. 1(b) is examined using the SPICE simulation program. In the simulations, the TSMC 0.35 μm level-3 SPICE parameters were used that are listed in Tab. 2 [25]. The aspect ratios of the MOS transistors are given in Tab. 3. The DC supply voltages are $\pm$2.5 V and the biasing current is 400 μA. The voltage and current characteristics of the introduced DCCII are given in Fig. 3. Main parameters of the proposed DCCII are summarized in Tab. 4.

```
.MODEL CMOSN NMOS (LEVEL = 3 TOX = 7.9E–9 NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549
+ DELTA = 0 UO = 436.256147 ETA = 0 THETA = 0.1749684 KP = 2.055786E–4 VMAX = 8.309444E4 KAPPA = 0.2574081
+ RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E–7 LD = 3.162278E–11 WD = 7.046724E–8 CGDO = 2.82E–10
+ CGSO = 2.82E–10 CGBO = 1E–10 CJ = 1E–3 PB = 0.9758533 MJ = 0.3448504 CJSW = 3.777852E–10 MJSW = 0.3508721)
.MODEL CMOSP PMOS (LEVEL = 3 TOX = 7.9E–9 NSUB = 1E17 GAMMA = 0.4083894 PHI = 0.7 VTO = –0.7140674
+ DELTA = 0 UO = 212.2319801 ETA = 9.999762E–4 THETA = 0.2020774 KP = 6.733755E–5 VMAX = 1.181551E5 KAPPA = 1.5
+ RSH = 30.0712458 NFS = 1E12 TPG = –1 XJ = 2E–7 LD = 5.000001E–13 WD = 1.249872E–7 CGDO = 3.09E–10
+ CGSO = 3.09E–10 CGBO = 1E–10 CJ = 1.419508E–3 PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E–10 MJSW = 0.5)
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Tab. 2. TSMC 0.35 μm level-3 CMOS parameters [25].

PMOS Transistors	W(μm)	L(μm)
M_3, M_4, M_{19}, M_{20}	60	0.35
M_5–M_7	30	2
M_{12}, M_{13}, M_{16}	30	1
M_{17}	60	2
NMOS Transistors	**W(μm)**	**L(μm)**
M_1, M_2, M_{18}, M_{21}	20	0.35
M_8, M_9	10	2
M_{10}, M_{11}, M_{14}	10	1
M_{15}	20	2

Tab. 3. Aspect ratio of the MOS transistors in DCCII.

Parameter	Value
Linearity v_{XN}/v_Y, v_{XP}/v_Y (V)	both –1.23 → 1.13
Linearity i_Z/i_{XN}, i_Z/i_{XP} (mA)	–0.75 → 0.96, –2.77 → 2.23
v_{XN}/v_Y, v_{XP}/v_Y gains (β_N, β_P)	both 0.983
i_Z/i_{XN}, i_Z/i_{XP} gains (α_N, α_P)	1.074, 1.087
v_{XN}/v_Y, v_{XP}/v_Y f_{-3dB} (GHz)	both 7.2
i_Z/i_{XN}, i_Z/i_{XP} f_{-3dB} (MHz)	350, 432

Tab. 4. Main parameters of the proposed DCCII given in Fig. 1(b).

The simulations shows that the current gain α_N of the DCCII a bit alters from α_P while the voltage gains β_N and β_P are equal. The f_{-3dB} frequency of voltage transfers is significantly higher than cut-off frequency of the current transfers.

The passive element values of the all-pass filter in Fig. 2 were chosen as $R_1 = 2$ kΩ, $R_2 = 8$ kΩ, and $C = 200$ pF to obtain a phase shift of 90° at pole frequency of $f_0 \approx 398$ kHz. The phase and gain responses of the all-pass filter are illustrated in Fig. 4. The total harmonic distortion (THD) variation with respect to amplitude of the applied sinusoidal input voltage at the pole frequency of the all-pass filter is shown in Fig. 5. The THD rapidly increases when the input signal is increased beyond 0.85 V amplitude. An input with the amplitudes of 0.3 V, 0.6 V, and 0.9 V yields THD values of 0.029 %, 0.051 %, and 0.623 %, respectively. The total power dissipation of the circuit is found as 14.3 mW. Moreover, using the INOISE and ONOISE statements, the input and output noise behavior with respect to frequency has also been simulated, as it is shown in Fig. 6. The equivalent input and output noises at $f_0 \approx 398$ kHz are found as 43.29 and 39.37 nV/$\sqrt{\text{Hz}}$, respectively.

The SPICE simulations confirm the feasibility of the proposed circuit and results are in good agreement with theory. Note that the inconsistencies in magnitude and phase characteristics are due to the non-idealities discussed in Section 3.

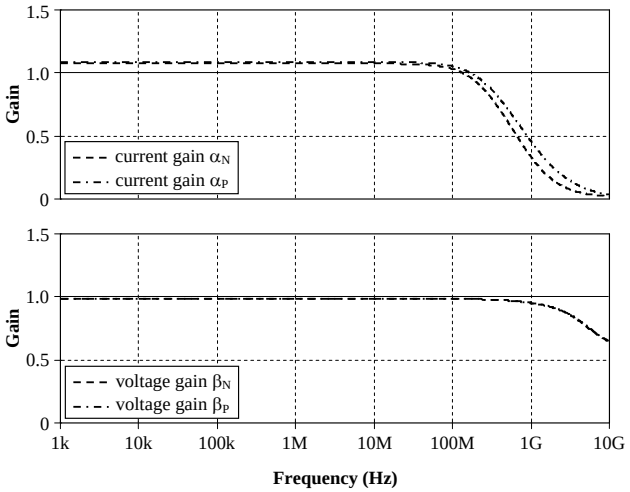

Fig. 3. Characteristics of the proposed DCCII implementation.

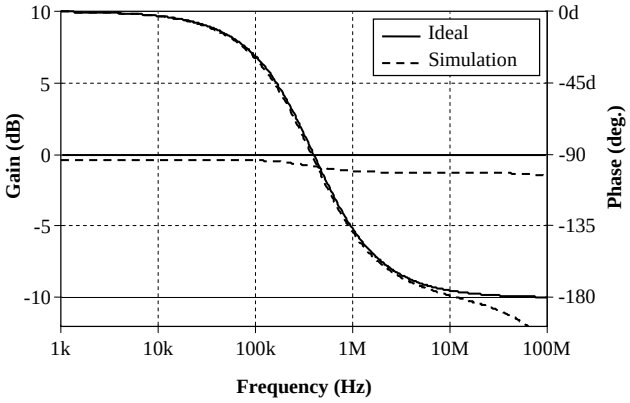

Fig. 4. Ideal and simulated gain and phase responses for the presented first-order all-pass filter.

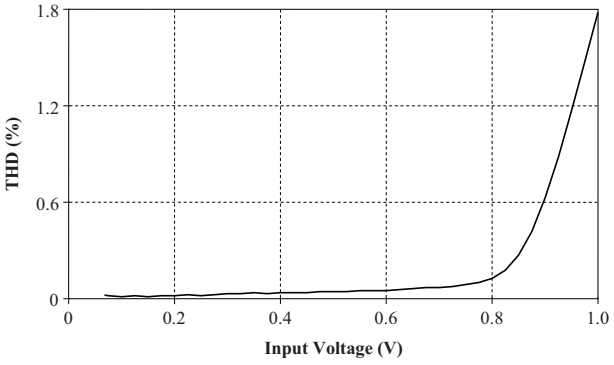

Fig. 5. THD variations versus amplitudes of the applied sinusoidal input voltages at $f_0 \approx 398$ kHz.

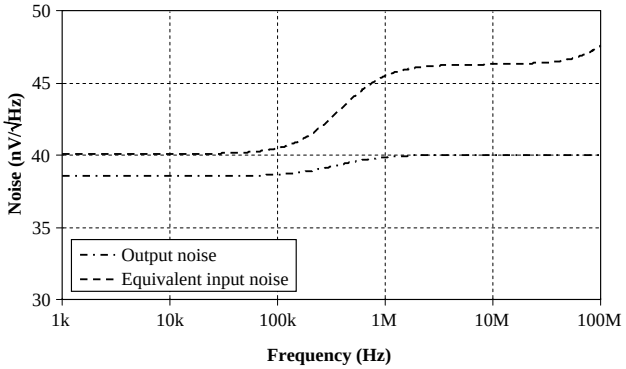

Fig. 6. Input and output noise variations versus frequency.

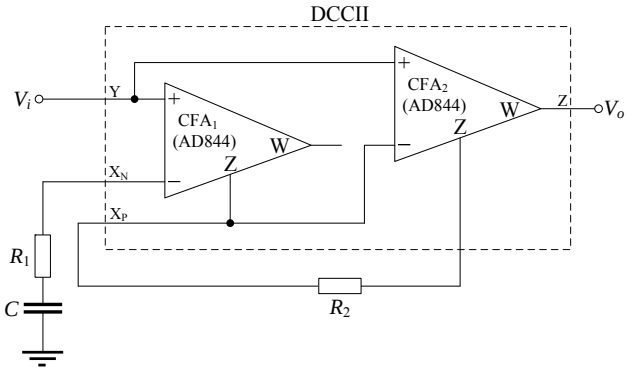

Fig. 7. Realization of the proposed circuit with a DCCII that includes of two AD844s for the experiment.

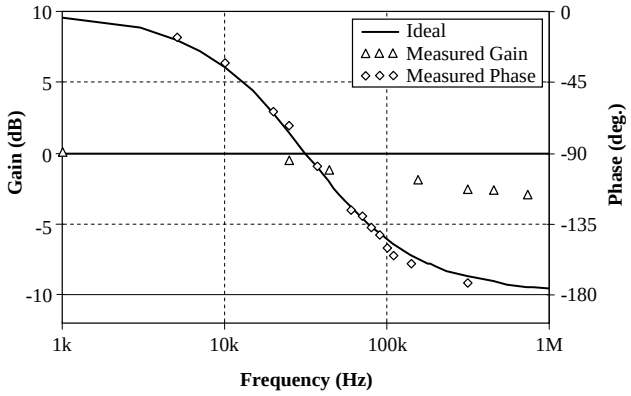

Fig. 8. Ideal and measured all-pass gain and phase responses.

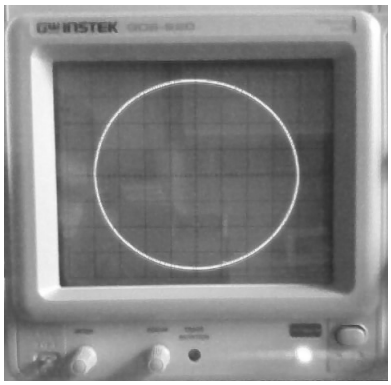

Fig. 9. The photograph of the experimental result for Lissajous ellipse at the pole frequency (horizontal and vertical scales are 0.2 V/division).

5. Experimental Results

In order to confirm the simulation results, the behavior of the proposed APF has also been verified by experimental measurements. The DCCII in Fig. 7 employs two commercially available CFAs AD844 ICs. Here should be noted that the output circuitry of CFA is voltage buffer. Hence, using the full potential of the CFA_2, the proposed APF has both high-input and low-output impedances, simultaneously. The supply voltages are $V_{DD} = -V_{SS} = 12$ V. The proposed APF with a pole frequency of $f_0 \cong 31.8$ kHz is designed with passive element values of $R_1 = 500\ \Omega$, $R_2 = 2$ kΩ, $C = 10$ nF, and the results are shown in Fig. 8. Note that the passive element tolerances are 2 % and 5 %, respectively. In addition, input and output signals at the pole frequency have also been applied to the oscilloscope in X-Y mode and the phase relationship between the signals is presented as a Lissajous ellipse. In the oscilloscope photography shown in Fig. 9, the horizontal and vertical scales are 0.2 V/division. Experimental results confirmed the theoretical results.

6. Conclusions

In this study, a new CMOS DCCII implementation is proposed. Usefulness of the DCCII is shown in a novel all-pass filter circuit. The presented filter has a high-impedance input and a grounded capacitor. Moreover, the measured APF has low-output impedance as well. Simulation and experimental results are given to verify the theory.

7. Appendix

This section provides full nomenclature of the aforementioned ABBs in Tab. 1.

CCII+(−):	Plus-type (minus-type) second-generation current conveyor
CCCII−:	Minus-type second-generation current-controlled current conveyor
CCIII−:	Minus-type third-generation current conveyor
DO-CCII:	Dual-output second-generation current conveyor
MCCII−:	Minus-type modified second-generation current conveyor
DVCC+:	Plus-type differential voltage current conveyor
DDCC+:	Plus-type differential difference current conveyor
FDCCII:	Fully differential current conveyor
VD-DIBA:	Voltage differencing-differential input buffered amplifier
C-(I)CDBA:	Current-controlled (inverting) current differencing buffered amplifier
UVC:	Universal voltage conveyor
DCCII:	Differential current conveyor

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About Authors...

Bilgin METIN received the B.Sc. degree in Electronics and Communication Engineering from Istanbul Technical University, Istanbul, Turkey in 1996 and the M.Sc. and Ph.D. degrees in Electrical and Electronics Engineering from Bogazici University, Istanbul, Turkey in 2001 and 2007 respectively. He is currently an Assistant Professor in the Management Information Systems Department of Bogazici University. His research interests include continuous time filters, analog signal processing applications, current-mode circuits, and information systems. He was given the best student paper award of ELECO'2002 conference in Turkey. He has over 25 articles in SCI and SCI-E indexed journals and 25 conference proceedings.

Norbert HERENCSAR received the M.Sc. and Ph.D. degrees in Electronics & Communication and Teleinformatics from Brno University of Technology, Czech Republic, in 2006 and 2010, respectively. Currently, he is an Assistant Professor at the Department of Telecommunications, Faculty of Electrical Engineering and Communication, Brno University of Technology, Brno, Czech Republic. From September 2009 through February 2010 he was an Erasmus Exchange Student with the Department of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey. His research interests include analog filters, current-mode circuits, tunable frequency filter design methods, and oscillators. He is an author or co-author of 20 research articles published in SCI-E international journals, 20 articles published in other journals, and 52 papers published in proceedings of international conferences. His paper "Generalized design method for voltage-controlled current-mode multifunction filters", presented and published at the 16th Telecommunications Forum TELFOR 2008, Belgrade, Serbia, was recommended for "Blazo Mircevski" Award granted for the best paper of a young TELFOR author. In 2011, he received Rector Award in the University competition "Top 10 Excelence VUT 2010" for the 9th most productive scientist at the Brno University of Technology, category "Publications". His paper "Novel resistorless dual-output VM all-pass filter employing VDIBA", presented and published at the 7th International Conference on Electrical Electronics Engineering - ELECO 2011, Bursa, Turkey, received "The best paper award in memory of Prof. Dr. Mustafa Bayram".

Since 2008, Dr. Herencsar serves in the organizing and technical committee of the International Conference on Telecommunications and Signal Processing (TSP). In 2011, he is guest co-editor of TSP 2010 Special Issue on Telecommunications, published in the Telecommunication Systems journal of Springer. In 2011 and 2012, he is guest co-editor of TSP 2010 and TSP 2011 Special Issues on Signal Processing, published in the Radioengineering journal. Dr. Herencsar is a Member of IEEE, ACEEE, IAENG, and Senior Member of IACSIT.

Kamil VRBA received the Ph.D. degree in Electrical Engineering in 1976, and the Prof. degree in 1997, both from the Technical University of Brno. Since 1990 he has been Head of the Department of Telecommunications, Faculty of Electrical Engineering and Computer Science, Brno University of Technology, Brno, Czech Republic. His research work is concentrated on problems concerned with accuracy of analog circuits and mutual conversion of analog and digital signals. In cooperation with AMI Semiconductor Czech, Ltd. (now ON Semiconductor Czech Republic, Ltd.) he has developed number of novel active function blocks for analog signal processing such as universal current conveyor (UCC), universal voltage conveyor (UVC), programmable current amplifier (PCA), digitally adjustable current amplifier (DACA), and others. He is an author or co-author of more than 700 research articles published in international journals or conference proceedings. Professor Vrba is a Member of IEEE and IEICE.